12-27-99 A

Please type a plus sign (+) inside this box → +

PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.p7651
First Inventor or Application Identifier	David W. Frame
Title	APPARATUS AND METHOD FOR COUPLING TO A MEMORY MODULE
Express Mail Label No.	EL034433694US

jc520 U.S. PTO 09/470542 12/22/99

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification [Total Pages 17]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) *(35 U.S.C. 113)* [Total Sheets 3]

4. Oath or Declaration [Total Pages 5]
a. ☐ Newly executed (original copy)
b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
9. ☐ English Translation Document *(if applicable)*
10. ☐ Information Disclosure Statement (IDS)/PTO - 1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. ☐ *Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
14. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. ☐ Other: .....

16. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: _____
Prior application Information: Examiner _____ *Group/Art Unit:* _____
For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

☐ *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or ☒ *Correspondence address below*

Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
Address	12400 Wilshire Boulevard, Seventh Floor				
City	Los Angeles	State	California	Zip Code	90025
Country	U.S.A.	Telephone	(503) 684-6200	Fax	(503) 684-3245

Name (Print/Type)	Aloysius TC. AuYeung, Reg. No. 35,432
Signature	[signature] Date 12/22/99

Burden Hour Statement. This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

APPARATUS AND METHOD FOR COUPLING TO A MEMORY MODULE

Inventor(s): David W. Frame
Christopher J. Banyai
Karl H. Mauritz
Albert R. Nelson
Qing-lun Chen
Hany M. Fahmy

Prepared by: Kenneth M. Seddon,
Patent Attorney

intel®
Intel Corporation
5000 W. Chandler Blvd., CH6-404
Chandler, AZ 85226-3699
Phone: (480) 554-9732
Facsimile: (480) 554-7738

"Express Mail" label number EL034433694US

APPARATUS AND METHOD FOR COUPLING TO A MEMORY MODULE

BACKGROUND

Within some computing systems, integrated circuits (e.g., processors and memory devices) may have a need to interact with each other, even though the integrated circuits may be physically located on different printed circuit boards. A technique to communicatively couple integrated circuits that are on different boards has been proposed by Rambus, Inc. of Mountain View, CA. The "Direct RAC Data Sheet," dated August 7, 1998 and available at http:// www.rambus.com/developer/support_asic.html, describes how a Direct Rambus™ ASIC Cell (Direct RAC) module may be used to control the transmission of data between a processor and a memory module. See also, "Direct Rambus Clock Generation Validation" version 1.0, July 1999, available at http://www.rambus.com.

The processor may include a RAC module that controls communication over a Rambus Channel that may comprise a plurality of lines. In the Rambus specification, each line in the Rambus Channel has an impedance value of 28 Ohms. The specification also provides for the use of connectors to connect a memory module to a printed circuit board containing a processor. However, the currently available connectors that may be used to connect memory modules to the Rambus Channel place the memory module at a right angle relative to the channel. Consequently, the memory modules extend at a right angle from the printed circuit board that contains the processor.

Although this configuration may be well suited to desktop applications, conventional implementations in accordance with the Rambus specification are not well

suited for applications that have small form factors, for example, portable computing applications. Moreover, the current Rambus specification specifies that the Rambus Channel is to have an impedance value of 28 Ohms. This specification may impose a limitation on the number of memory modules or repeater hubs that may be coupled to the Rambus Channel due to fan-out issues.

Thus, there is a continuing need for better ways to communicatively couple processors to memory modules.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

FIG. 1 is a block diagram representation of an embodiment of a system having a communication bus in accordance with the present invention;

FIG. 2 is a sectional representation of a memory mezzanine and a printed circuit board in accordance with an embodiment of the present invention; and

FIG. 3 is a sectional representation of a connector in accordance with an embodiment of the present invention.

It will be appreciated that for simplicity and clarity of illustration, elements

illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

FIG. 1 is a block diagram representation of a computing system 10 in accordance with an embodiment of the present invention. Computing system 10 may be a variety of apparatuses, including without limitation, a portable computing system, a desktop computing system, and the like. Computing system 10 may include a computing board 11 that is communicatively coupled to a memory mezzanine 20. Memory Mezzanine 20 may comprise storage mediums that are accessed by a processor, and may be, for example, a memory expansion module, a memory card, and the like, although the scope of the present invention is not limited to these examples. Computing board 11 may include a variety of integrated circuits, such as a processor 12, that are coupled to a memory controller hub (MCH) 13. In this embodiment, MCH 13 may be an 82840® processor, which is available from Intel Corporation, Santa Clara, CA.

MCH 13 may assume responsibility for sending and receiving data between

processor 12 and memory mezzanine 20. Although this is not intended to be a limitation of the scope of the present invention, MCH 13 may include a Rambus ASIC Cell (RAC) 14, such as a Direct Rambus™ Rambus ASIC Cell that serves as a communication controller. It should be understood that the scope of the present invention is not limited to computing systems that implement the Rambus communication protocol. Alternative communication modules may be used to control the exchange of data signals between a processor and a storage medium, such as a disk drive, memory module, or the like, that may or may not be Rambus™ compatible.

Memory mezzanine 20 may also include a variety of integrated circuits such as a memory repeater hub (MRH) 21 that may be coupled to memory device(s) 25. As shown, MRH 21 may include a RAC 22 that is communicatively coupled to RAC 14 so that data and instructions may be exchanged between computing board 11 and memory mezzanine 20. The process and protocols for exchanging information are provided in the aforementioned Rambus "Direct RAC Data Sheet."

In this embodiment, memory mezzanine 20 includes a plurality of memory devices 25 that may be used by processor 12 to store data. Although the scope of the present invention is not limited in this respect, memory devices 25 may be, for example, a Rambus Dynamic Random Access Memory (RDRAM), a Rambus In-Line Memory Module (RIMM), a Dual In-Line Memory Module (DIMM), a Synchronous-clocked Dynamic Random Access Memory (SDRAM), Double Data Rate DRAM (DDR), another MRH, etc.

A bus 15 may communicatively couple RAC 14 to a RAC 22. In this embodiment, bus 15 comprises a dual-terminated transmission line that may include one or more signal lines that are used by MCH 13 and MRH 21 to exchange data. For example, as specified

by the Rambus standard, bus 15 may comprise multiple lines that communicate signals such as data signals, clock signals, parity signals, reset signals, handshaking signals, and the like. It should, however, be appreciated that the scope of the present invention is not limited to transmitting signals of only this or any other type. Typically, bus 15 has at least 10 signal lines and may have 32 lines as dictated by the Rambus specification.

In this embodiment, bus 15 may included at least two resistors 18, one adjacent to each of computing board 11 and memory mezzanine 20, respectively. Resistors 18 are positioned near the ends of bus 15 to reduce the amount of reflection that occurs when communication/transmission signals reach the either end of bus 15. The resistance value of resistors 18 may be determined by a variety of parameters such as the impedance of bus 15, the clock rate at which data is broadcasted over bus 15, the relative strength of the data signals, and the sensitivity of RAC's 14 and 22. Resistors 18 may have a resistance value ranging from approximately 25 ohms to 65 ohms so that the resistance value of resistors 18 is about 7-12% higher or lower than the impedance value of bus 15. In one embodiment, bus 15 may have an impedance value of about 50 Ohms and resistors 18 may have a resistance value of about 55 Ohms. However, the scope of the present invention is not limited to the values recited above as bus 15 may have an impedance ranging from about 45 Ohms to 55 Ohms, or even, 45 Ohms to 65 Ohms. Furthermore, embodiments of the present invention may be used in computing systems where the impedance of bus 15 is about 28 Ohms, or has an impedance value ranging from about 25 ohms to 25 ohms.

Conventional Rambus specifications require that the impedance of the bus lines be about 28 Ohms, which as explained above, may serve to limit the data rate and fan-out of

memory devices that may be coupled to the bus. However, the bus of this embodiment of the present invention addresses at least some of these limitations. This embodiment, for example, may be used to provide source-synchronous communication between two devices at data rates that are much faster than may have been previously possible. For example, bus 15 is adapted to provide a clock signal at a rate in excess of 250 MHz, and is well-suited to provide a clock signal at a rate ranging from about 300 MHz to 400 MHz, and even, about 300 MHz to 800 MHz. With these clock speeds and data bus widths, it may be possible to transmit data signals across bus 15 at a rate in excess of 1 Gbytes/sec, for example.

In the embodiment illustrated in FIG. 1, RAC's 14 and 22 are directly connected together by bus 15. However, it should also be understood that in alternative embodiments of the present invention, it is possible to use a connector(s) to couple computing board 11 and memory mezzanine 20. As shown in FIG. 2, a connector 51 may be used to couple computing board 11 to memory mezzanine 20. FIG. 2 is also provided to illustrate examples of how memory devices 25 may be coupled to memory mezzanine 20. As shown, a connector 56 may be used to connect a memory device 25 at a right angle to memory mezzanine 20, or a memory device 25 may be directed mounted onto memory mezzanine 20. Likewise, a connector 57 may be used to connect memory device 25 at an angle relative to memory mezzanine 20. Although not shown, in alternative embodiments, memory devices 25 may be directly mounted to computing board 11 using one of the same or similar techniques used to connect to memory mezzanine 20.

FIG. 3 is a sectional view of connector 57, which may be desirable in applications

that have small form factors, e.g., portable computers. As indicated with brackets 70 and 71, a portion (e.g., the portion indicated by bracket 70) of connector 57 is at an angle 100 relative to the body of connector 57 (e.g., the portion indicated by bracket 71). The magnitude of angle 100 may vary depending on the overall height desired for connector 57 and memory device 25. Connector 57 may be formed so that memory device 25 is at an angle of about 25 degrees relative to the surface of memory mezzanine 20. Furthermore, angle 100 may range from about 30 degrees to 40 degrees.

Connector 57 may include metal lines 60 and 61 that are used to communicatively couple to memory device 25. Although only two metal lines are shown in FIG. 3, the number of metal lines should not be considered a limitation of the present invention as the number of metal lines may increase, as desired, to provide communication with memory device 25. As shown in FIG. 3, metal line 61 is longer than metal line 62 as a result of the angle of connector 57. It has been discovered that slight variations in the length of each of the metal traces may significantly impact the amount of reflections that occur when data is transmitted to or received from memory device 25. This in turn, may impact the maximum rate at which data may be transferred through a connector.

Although a variation in impedance may be insignificant when data is transmitted at 100 MHz or less, the variation in impedance may become a severe limiting factor for data transfer rates of 200-400 MHz and becomes even more significant of a problem as the data rate approaches 800 MHz. In accordance with an aspect of the present invention, one technique for addressing the mismatch in the length of metal lines 60 and 61 is to increase the natural, parasitic capacitance value of the longer line, e.g., metal line 61. As shown by the formula, impedance = (inductance/capacitance)$^{1/2}$, the impedance of a metal

line is directly proportional to the inductance of the line and inversely proportional to the capacitance of the line.

Therefore, any increase in the inductance of metal line 61 due to its additional length, may be offset by a proportionately equal increase in the capacitance value of the same line. The capacitance of metal line 61 may be increased in a variety of ways including, without limitation, by adjusting the physical shape of metal line 61, by adjusting the materials used to form metal line 61, by adjusting the property of the materials surrounding metal line 61, or by adding a discrete capacitor to metal line 61. By making the parasitic capacitance value of metal line 61 greater than the parasitic capacitance value of metal line 60, the impedance of metal line 61 may be reduced so that the impedance of metal line 61 may be substantially equal to the impedance of metal line 60. Thus, this embodiment of the present invention is contrary to the teachings of the art that call for minimizing the parasitic capacitance of any conductive line.

The speed at which data may be transmitted over data lines is dependent in part on any variation in impedance between lines that are used to transmit similar data. This becomes more of a concern as the data transfer rate is increased. Up to now, the problem in mismatched impedance has not been a significant issue because traditional data transfer rates of 66 MHz, 100 MHz, or 133 MHz are not significant enough to cause computing system to suffer from this problem. However, as data transfer rates approach upwards of 800 MHz, the problem may become more significant with angled connectors, and thus, the advantages of the embodiments of the present invention may become more apparent.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those

skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

Claims:

1. An apparatus comprising:

a first integrated circuit comprising a Direct Rambus™ ASIC Cell (Direct RAC);

a second integrated circuit comprising a Direct RAC; and

a dual-terminated transmission line, wherein the dual-terminated transmission line communicatively couples the Direct RAC of first integrated circuit with the Direct RAC of the second integrated circuit.

2. The apparatus of claim 1, wherein the dual-terminated transmission line includes a first resistor adjacent to the first integrated circuit and a second resistor adjacent to second integrated circuit.

3. The apparatus of claim 2, wherein the first resistor and the second resistor have a resistance value ranging from approximately 25 ohms to 65 ohms.

4. The apparatus of claim 3, wherein the dual-terminated transmission line has an impedance value, and the resistance value of the first resistor is about 7-12% higher than the impedance value of the dual-terminated transmission line.

5. The apparatus of claim 3, wherein the dual-terminated transmission line has an impedance value of about 50 ohms, and the first resistor has a resistance value of about 55 ohms.

6. The apparatus of claim 1, wherein the second integrated circuit comprises a memory repeater hub.

7. The apparatus of claim 1, wherein the first integrated circuit and the second integrated circuit are adapted to provide source-synchronous communication between each other.

8. The apparatus of claim 1, wherein the dual-terminated transmission line is adapted to provide a clock signal at a rate in excess of 250 MHz.

9. The apparatus of claim 8, wherein the dual-terminated transmission line is adapted to provide a clock signal at a rate ranging from about 300 MHz to 800 MHz.

10. The apparatus of claim 1, further comprising:

a mezzanine card having a connector and comprising the second integrated circuit, wherein the connector is adapted to be communicatively coupled to a third integrated circuit.

11. The apparatus of claim 10, wherein the connector includes a first metal line and a second metal line, the second metal line being longer than the first metal line, and wherein the second metal line has a parasitic capacitance value greater than a parasitic capacitance value of the first metal line.

12. The apparatus of claim 11, wherein impedance of the first metal line is substantially equal to impedance of the second metal line.

13. The apparatus of claim 12, wherein the connector has a first portion and a second portion, the second portion being at an angle ranging from about 30 degrees to 40 degrees relative to the first portion.

14. The apparatus of claim 13, wherein the second portion is at an angle of about 25 degrees relative to the first portion.

15. The apparatus of claim 10, wherein the third integrated circuit comprises a Rambus™ in-line memory module communicatively coupled to the connector.

16. An article comprising:

a memory module including a connector that is adapted to be coupled to a first integrated circuit; and

wherein the connector has a first line and a second line, the second line being longer than the first line, the second line having a capacitance value greater than a capacitance value of the first line, and wherein impedance of the second line is approximately equal to impedance of the first line.

17. The article of claim 16, further comprising:

a second integrated circuit; and

a transmission line adapted to communicatively couple the first integrated circuit and the second integrated circuit, wherein the transmission line has an impedance value ranging from about 25 ohms to 35 ohms.

18. The article of claim 16, further comprising:

a second integrated circuit; and

a dual-terminated transmission line adapted to communicatively couple the first integrated circuit and the second integrated circuit.

19. A method of making an article, comprising:

providing a first integrated circuit having a communication module;

providing a second integrated circuit have a communication module; and

forming a dual-terminated transmission line to couple the first integrated circuit to the second integrated circuit.

20. The method of claim 19, further comprising providing a connector having a first line and a second line, wherein the first line and the second line are communicatively coupled to the first integrated circuit, and wherein the second line is longer than the first line, has a capacitance value greater than a capacitance value of the first line, and impedance of the second line is approximately equal to impedance of the first line.

Express Mail Label No. EV339050426US

21. A method of communicating between a first integrated circuit and a second integrated circuit, comprising:

providing a dual-terminated transmission line communicatively coupling the first integrated circuit and the second integrated circuit; and

transmitting data signals across the dual-terminated transmission line at a rate in excess of 1 Gbytes/sec.

22. The method of claim 21, wherein providing a dual-terminated transmission line includes providing a dual-terminated transmission line having an impedance ranging from about 45 Ohms to 55 Ohms.

APPARATUS AND METHOD FOR COUPLING TO A MEMORY MODULE

Abstract

Briefly, in accordance with one embodiment of the invention, a system includes two boards coupled by a bus. The bus having a dual-terminated transmission line that communicatively couples a memory control hub with a memory repeater hub that each have a Rambus ASIC Cell (RAC). Briefly, in accordance with another embodiment of the invention, a connector has two metal traces that are of different lengths. The parasitic capacitance of the longer metal trace is increased so that the impedance of the two metal traces is substantially equal.

662221 24502400

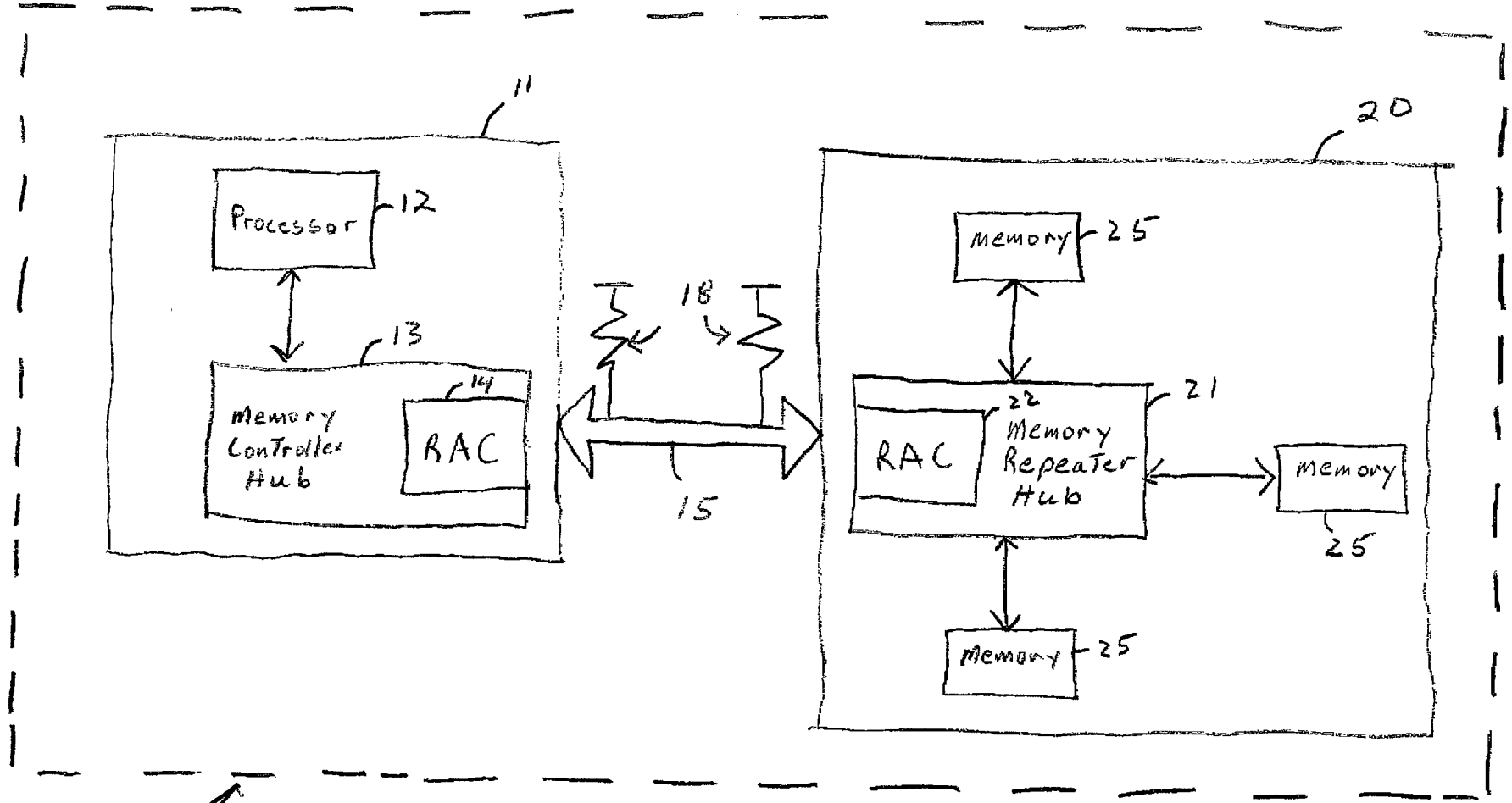


FIG. 1

42390.P7651

DEC-22-1999 09:20 FROM INTEL LEGAL & FINANCE TO 915036843245 P.02/04
DEC 22 '99 09:18AM
22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

09422221 "2450260

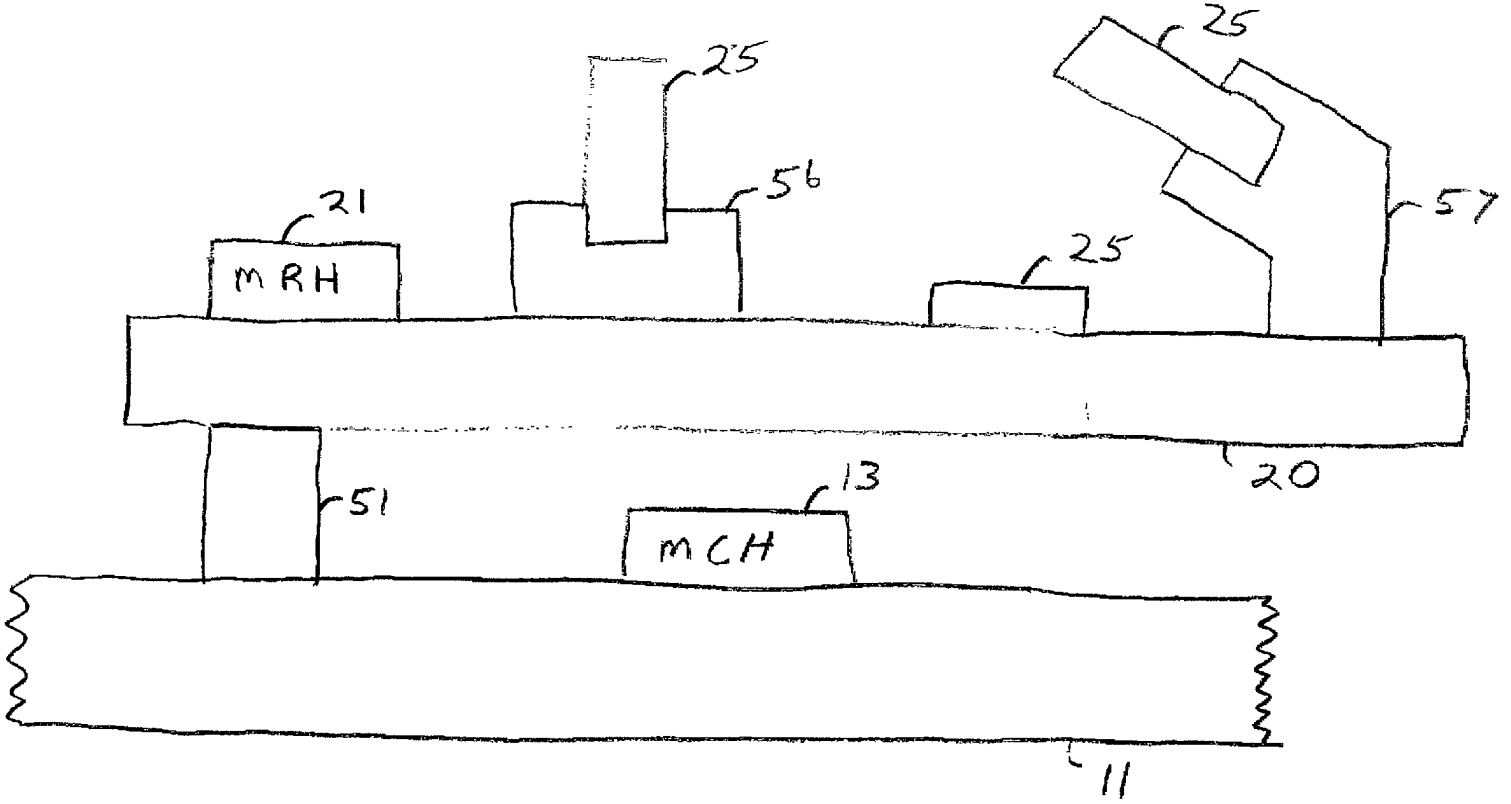


FIG. 2

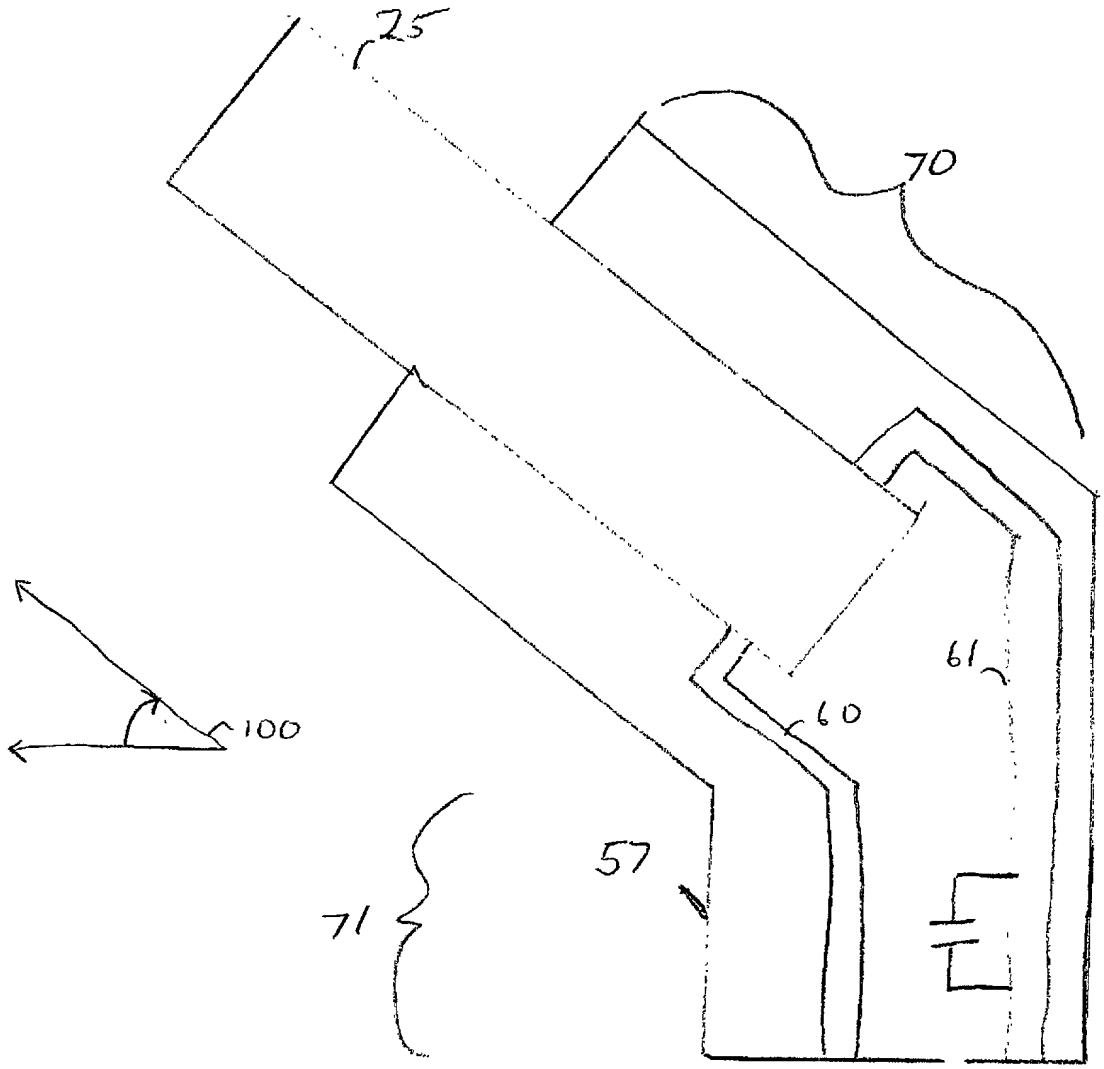
42390.P7651

DEC-22-1999 09:20 FROM INTEL LEGAL & FINANCE TO 915036843245 P.03/04
DEC 22 '99 09:18AM

AMPAD
22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS

P42390.P765

FIG 3



22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

APPARATUS AND METHOD FOR COUPLING TO A MEMORY MODULE

the specification of which

[X] is attached hereto.
[ ] was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____ .
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, a firm including: William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. 44,587; Thomas M. Coester, Reg. No. 39,637; Donna Jo Coningsby, Reg. No. 41,684; Stephen M. De Klerk, under 37 C.F.R. § 10.9(b); Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Erica W. Kuo, Reg. No. 42,775; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Lisa A. Norris, Reg. No. P44,976; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Kimberley G. Nobles, Reg. No. 38,255; Daniel E. Ovanezian, Reg. No. 41,236; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. P45,241; Steven D. Yates, Reg. No. 42,242; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; Paramita Ghosh, Reg. No. 42,806; and Sang Hui Kim, Reg. No. 40,450; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. P44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Aloysius T.C. AuYeung, Reg. No. 35,432, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Aloysius T.C. AuYeung, Reg. No. 35,432, (503) 684-6200.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor (given name, family name) **David W. Frame**

Inventor's Signature _____ Date _____

Residence Aloha, Oregon USA Citizenship USA
(City, State) *(Country)*

P. O. Address 6815 SW 203rd Ct.

Aloha, Oregon 97007 USA

Full Name of Second/Joint Inventor (given name, family name) **Christopher J. Banyai**

Inventor's Signature _____ Date _____

Residence Chandler, Arizona Citizenship USA
(City, State) *(Country)*

P. O. Address 1902 W. Bluebird Drive

Chandler, Arizona 85248

Full Name of Third/Joint Inventor (given name, family name) **Karl H. Mauritz**

Inventor's Signature _____ Date _____

Residence Chandler, Arizona USA Citizenship USA
(City, State) *(Country)*

P. O. Address 444 n. Gila Springs Blvd.

Chandler, Arizona 85226 USA

Full Name of Fourth/Joint Inventor (given name, family name) **Albert R. Nelson**

Inventor's Signature _____ Date _____

Residence Olympia, Washington USA Citizenship USA
(City, State) *(Country)*

P. O. Address 4426 36th Ave., NE

Olympia, Washington 98516 USA

Full Name of Fifth/Joint Inventor (given name, family name) **Quing-Lun Chen**

Inventor's Signature _____ Date _____

Residence Lakewood, Washington USA Citizenship China
(City, State) *(Country)*

P. O. Address 9508 56th Ave., SW EE202#

Lakewood, Washington 98499 USA

Full Name of Sixth/Joint Inventor (given name, family name) **Hany M. Fahmy**

Inventor's Signature _____ Date _____

Residence University Place, Washington USA Citizenship Canada
(City, State) *(Country)*

P. O. Address 8615 26th Street, West, Apt. #231

University Place, Washington 98466 USA

Full Name of Seventh/Joint Inventor (given name, family name)

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) *(Country)*

P. O. Address _____

_____

Full Name of Eighth/Joint Inventor (given name, family name)

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) *(Country)*

P. O. Address _____

_____

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.